channel every 2n samples.--

REMARKS

Claims 1, 3-7, and 9-13 remain in the application and have been amended hereby.

As will be noted from the Declaration, Applicants are citizens and residents of Japan and this application originated there.

Accordingly, the amendments to the specification are made to place the application in idiomatic English, and the claims are amended to place them in better condition for examination.

An early and favorable examination on the merits is earnestly solicited.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure has been amended as follows:

--[The present invention provides a] A digital signal encoding apparatus for encoding one-bit signals of a plurality of n ($n \geq 2$) channels [which] that is modulated in [the] a delta-sigma manner, [which includes] including a channel compositor 6 for compositing scrambled data supplied from [the] a first scrambler [L 4] and scrambled data supplied from [the] a second scrambler [R 5], a phase modulator 7 for phase-modulating composited data supplied from the channel compositor 6, a SYNC signal adding and correcting unit 8 for receiving SYNC timing signals generated at and supplied from a SYNC timing generator 9 and inserting SYNC signals into phase-modulated one-bit audio signal data supplied from the phase modulator 7 to generate SYNC patterns and correct the SYNC patterns, and an information data adding unit 11 for adding information data which is related with one-bit audio signals to phase-modulated one-bit audio signal data via the SYNC signal adding and correcting unit 8 by rearranging data of inverted phases thereof based on [the basis of] a two channel unit.--

IN THE CLAIMS

Claims 1, 3-7, and 9-13 have been amended as follows:

--1. (Amended) A digital signal encoding apparatus for encoding one-bit signals of a plurality of n [(n≥2)] channels, n being equal to at least two, and the one-bit signals being modulated in [the] a delta-sigma manner, the apparatus comprising:

phase modulating means for phase-modulating the one-bit signals as original signals to add data of inverted phases [thereto] to the one-bit signals; and

information data adding means for adding information data [which is] that are related [with] to the one-bit signals to the phase-modulated one-bit signal data having the data of inverted phases added [thereto] by rearranging the data of inverted phases based on [the basis of] a plurality of m [(n≥m≥2)] channel [unit] units of the n channels, wherein n≥m≥2.

--3. (Amended) The digital signal encoding apparatus as set forth in Claim 2, wherein[, in case] when the m is equal to 2 and two-bit data of the phase-modulated one-bit signal data is [[0, 1] or [1, 0],] one of 0,1 and 1,0 the information data adding means rearranges the data of inverted phases in accordance with the information data.

--4. (Amended) The digital signal encoding apparatus as

set forth in Claim 3, wherein[, in case] when the information data is [[1],] 1 the information data adding means rearranges the data of inverted phases.

--5. (Amended) The digital signal encoding apparatus as set forth in Claim 1, further comprising synchronization signal adding means for adding independent synchronization patterns [which] that cannot exist in one of the phase-modulating means [or in] and the information data adding means by arranging a region of a plurality of samples other than a region to which the information data is added in the phase-modulated one-bit signal data every predetermined period[,] and converting the data of inverted phases in the region in accordance with the phase-modulated one-bit signal data.

--6. (Amended) The digital signal encoding apparatus as set forth in Claim 5, further comprising correcting means for making the numbers of one-bit data [[1]s] 1's and one-bit data [[0]s] 0's in the predetermined period[, which] that are generated when the synchronization patterns are added by the synchronization signal adding means[,] equal to each other by converting the data of inverted phases in a region of the predetermined period so that [the] a difference between the numbers of [[1]s and [0]s becomes] 1's and 0's is zero.

--7. (Amended) A digital signal encoding method for encoding one-bit signals of a plurality of n [(n≥2)] channels,

n being equal to at least two, and the one-bit signals being modulated in [the] a delta-sigma manner, the method comprising the steps of:

phase-modulating the one-bit signals as original signals to add data of inverted phases [thereto] to the one-bit signals;

adding information data [which is] that are related [with] to the one-bit signals to the phase-modulated one-bit signal data having the data of inverted phases added [thereto] by rearranging the data of inverted phases based on [the basis of] a plurality of m [(n≥m≥2)] channel [unit] units of the n channels, wherein n≥m≥2;

adding independent synchronization patterns [which] that cannot exist in one of the phase-modulating step [or in] and the information data adding step by arranging a region of a plurality of samples other than a region to which the information data [is] are added in the phase-modulated one-bit signal data every predetermined period[,] and converting the data of inverted phases in the region in accordance with the phase-modulated one-bit signal data; and

making [the] numbers of one-bit data [[1]s] 1's and one-bit data [[0]s] 0's in the predetermined period[, which] that are generated when the synchronization patterns are added by the synchronization signal adding step[,] equal to each other by converting the data of inverted phases in a region of the predetermined period [so] such that the difference between the numbers of [[1]s] 1's and [[0]s] 0's [becomes] is zero.

--9. (Amended) The digital signal encoding method as set forth in Claim 8, wherein[, in case] when the m is equal to 2 and two-bit data of the phase-modulated one-bit signal data is [[0, 1] or [1, 0],] one of 0,1 and 1,0 the information data adding step rearranges the data of inverted phases in accordance with the information data.

--10. (Amended) The digital signal encoding method as set forth in Claim 9, wherein[, in case] when the information data is [[1],] 1 the information data adding step rearranges the data of inverted phases.

--11. (Amended) A digital signal decoding apparatus for decoding a one-bit data stream transmitted from a digital signal encoding apparatus [which] that phase-modulates one-bit signals as original signals of a plurality of n [(n≥2)] channels to add data of inverted phases [thereto] to the one-bit signals, the one-bit signals being modulated in [the] a delta-sigma manner, and that adds information data [which is] that are related [with] to the one-bit signals to the phase-modulated one-bit signal data having the data of inverted phases added [thereto] by rearranging the data of inverted phases based on [the basis of] a plurality of m [(n≥m≥2)] channel [unit] units of the n channels to generate the one-bit data stream, where n≥m≥2, the digital signal decoding apparatus comprising:

synchronization signal detecting means for self-

extracting synchronization signals by detecting independent synchronization patterns [which] that cannot exist in the phase-modulating processing [or in] and the information data adding processing[,] and that are added by arranging a region of a plurality of samples other than a region to which the information data [is] are added in the one-bit data stream every predetermined period and converting the data of inverted phases in the region in accordance with the phase-modulated one-bit signal data;

information data detecting means for detecting the information data by judging [the] insertion positions of the data of inverted phases in the one-bit data stream based on the synchronization signals detected by the synchronization signal detecting means; and

judging means for judging original signal data in the one-bit data stream based on the synchronization signals detected by the synchronization signal detecting means[,] and for detecting the original signal data from leading data of each channel every 2n samples.

--12. (Amended) A digital signal decoding method for decoding a one-bit data stream transmitted from a digital signal encoding apparatus [which] that phase-modulates one-bit signals as original signals of a plurality of n [($n \geq 2$)] channels to add data of inverted phases [thereto] to the one-bit signals, the one-bit signals being modulated in [the] a delta-sigma manner, and adds information data [which is] that

are related [with] to the one-bit signals to the phase-modulated one-bit signal data having the data of inverted phases added [thereto] by rearranging the data of inverted phases on the basis of a plurality of m [(n≥m≥2)] channel [unit] units of the n channels to generate the one-bit data stream, where n≥m≥2 and the method comprising the steps of:

self-extracting synchronization signals by detecting independent synchronization patterns [which] that cannot exist in the phase-modulating processing [or in] and the information data adding processing[,] and that are added by arranging a region of a plurality of samples other than a region to which the information data is added in the one-bit data stream every predetermined period and converting the data of inverted phases in the region in accordance with the phase-modulated one-bit signal data;

detecting the information data by judging [the] insertion positions of the data of inverted phases in the one-bit data stream transmitted from a digital signal encoding apparatus based on the synchronization signals detected by the synchronization signal detecting step; and

judging original signal data in the one-bit data stream transmitted from a digital signal encoding apparatus based on the synchronization signals detected by the synchronization signal detecting step[,] and detecting the original signal data from leading data of each channel every 2n samples.

--13. (Amended) A digital signal transmitting system,

comprising:

a digital signal encoding apparatus [which] that phase-modulates one-bit signals as original signals of a plurality of n [(n≥2)] channels to add data of inverted phases [thereto], to the one-bit signals the one-bit signals being modulated in [the] a delta-sigma manner[,] and that adds information data [which is] that are related with the one-bit signals to the phase-modulated one-bit signal data having the data of inverted phases added [thereto] by rearranging the data of inverted phases based on [the basis of] a plurality of m [(n≥m≥2)] channel unit of the n channels to generate a one-bit data stream, wherein n≥m≥2; and

a digital signal decoding apparatus [which] that self-extracts synchronization signals by detecting independent synchronization patterns included in the one-bit data stream[, which] that cannot exist in the phase-modulating processing [or] and in the information data adding processing, and that detects the information data by judging the insertion positions of the data of inverted phases in the one-bit data stream based on the synchronization signals[,] and judges original signal data in the one-bit data stream based on the synchronization signals and detects the original signal data from leading data of each channel every 2n samples.--